I CLAIM

1. A system for synchronizing data streams, the system comprising:

a) an input source for a CLK and a SYNC stream;

b) a SYNC decoder for receiving said CLK and SYNC streams and decoding said SYNC stream packets into a qualified system time events;

c) a plurality of SYNC receivers, for receiving said qualified system time events and converting said qualified system time events to one or more derived time events; and

d) output means for transmitting said derived time events.

2. The system of claim 1 wherein said input source comprises one or more master locks.

3. The system of claim 1 wherein said input source comprises a locked oscillator.

4. The system of claim 1 wherein said input source comprises an external master reference.

5. The system of claim 1 wherein each of said SYNC receivers comprises a flywheeling counter.

6. The system of claim 1 wherein said SYNC stream comprises a plurality of packets, each packet comprising: a high level logic bit, a packet start bit, a group of flag bits, a low bit, a group of checkword bits; and a take bit.

7. The system of claim 6, wherein the flag bits, low bit and checkword bits may repeat within each packet.

8. A method for synchronizing data streams comprising the steps of:

a) receiving a CLK signal;

b) receiving a SYNC stream;

c) decoding said SYNC stream into a plurality of qualified system time events, said decoding utilizing said CLK signal;

d) transmitting each of said plurality of qualified system time events to one or more receivers;

e) creating and synchronizing derived time events contained in said qualified system time events packets within said receivers; and

f) transmitting said derived time events.

9. A method for synchronizing data streams, said method comprising:

a) receiving a CLK stream and a SYNC stream;

b) decoding said SYNC stream into qualified system time events;

c) transmitting said qualified system time events to a plurality of SYNC receivers,

d) converting of said qualified system time events by said SYNC receivers to one or more derived time events; and

e) transmitting said derived time events to one or more components.

10. The method of claim 9 wherein said CLK stream is received from one or more master locks.

11. The method of claim 10 wherein said one or more master locks receive said CLK stream from an external master reference.

12. The method of claim 9 wherein said CLK stream is received from a locked oscillator.

13. The method of claim 9 wherein said converting of said SYNC packets utilizes at least one flywheeling counter.

14. A computer data signal embodied in a transmission medium comprising:
a plurality of packets, each packet comprising: a high level logic bit, a packet start bit, a group of flag bits, a low bit, a group of checkword bits; and a take bit.

15. The data signal of claim 14, wherein the flag bits, low bit and checkword bits may repeat within each packet.

16. The data signal of claim 14 wherein said group of flag bits indicate video and audio synchronization events for the purpose of synchronizing an MPEG-2 data stream.